

S.Yamamura, N.Hidaka, Y.Tokumitsu, M.Fukuta
Fujitsu Laboratories Ltd.

ABSTRACT

A 4-8 GHz GaAs FET balanced amplifier has been constructed on a 4mm x 5mm sapphire substrate. Lumped elements used in microwave- and DC bias-circuits, and 3-dB coupler were fabricated on the substrate using thin film technology.

Introduction

Up to the present, wide-band GaAs FET amplifiers have been developed using distributed circuit elements, which can be fabricated on alumina substrates using thick film technology. Size of the amplifiers is relatively large since it depends on the wave length of operational frequency. Therefore, efforts for miniaturization, which will reduce size, weight and cost, have been continued.

We have developed a 4-8 GHz miniaturized GaAs FET balanced amplifier fabricated on a 4mm x 5mm sapphire substrate using thin film technology. A miniature amplifier was developed using simple matching circuits which were designed using computer technology.

This paper describes evaluation of lumped elements, design of a microwave amplifier, and performance of the miniaturized GaAs FET amplifier.

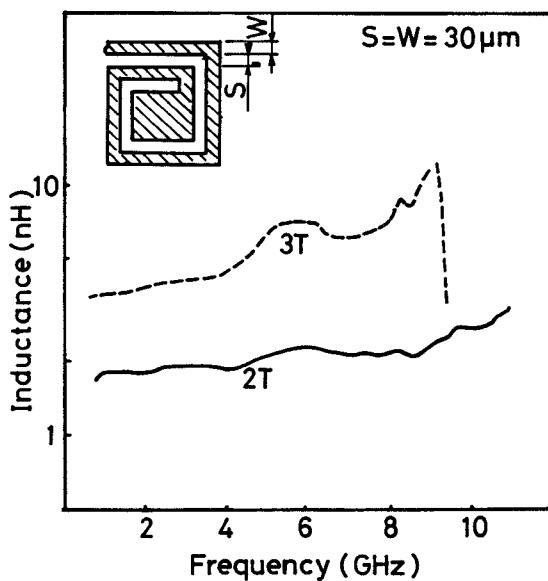


Figure 1. Frequency response of inductance of the spiral.

solid line --- 2-turn spiral
broken line--- 3-turn spiral

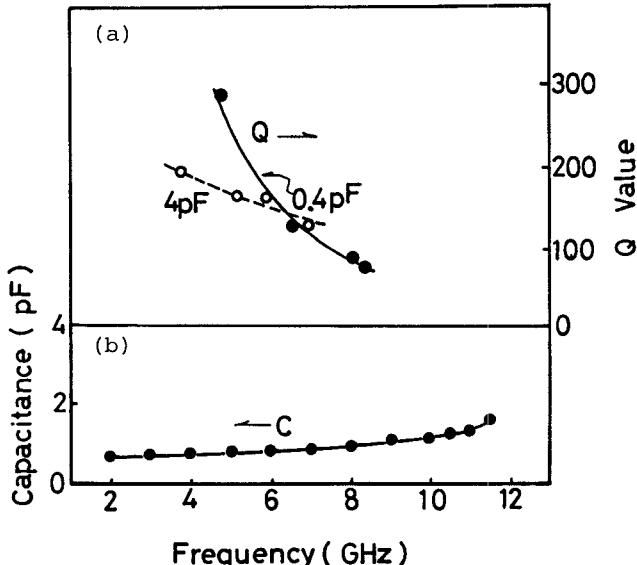


Figure 2. Frequency response of capacitance and quality factor (Q Value) of the MOM capacitor.

Evaluation of lumped elements

Passive elements used in the amplifier are spiral inductors, metal-oxide-metal (MOM) capacitors, thin-film resistors, and 3-dB hybrid couplers. Fig.1 shows the frequency response of inductance of the spiral. The line-width of the spiral inductors is 30 μm and is equal to these line-gap. The solid line and the broken line in Fig.1 show the inductance of the inductors used in a matching circuit and a bias circuit, respectively. Inductance of the former is constant over a frequency range of 2 to 9 GHz and this inductor is suitable for use in matching circuits. The self-resonant frequency of the latter is about 9.5 GHz. According to this and other experimental results, the self-resonant frequency of the spiral inductor is almost coincident with the frequency at which the spiral inductor's length is a quarter effective wave length. It seems that the coupling between lines of the spiral is weak.

The dielectric of the MOM capacitor con-

sists of a $0.5 \mu\text{m}$ silicon dioxide film deposited by a CVD of SiH_4 and O_2 . Fig.2 shows the frequency response of the capacitance and quality factor(Q Value) of the MOM capacitor. The capacitance of the capacitor for impedance matching in Fig.2(b) is constant over the frequency range of 1 to 12 GHz. The solid and broken lines in Fig.2 show Q values of capacitors having capacitance of 0.4 pF and 4 pF , respectively. Q value increases as the capacitance decreases at a low frequency when the thickness of a dielectric film is constant. But these lines in Fig.2(a) cross each other. The reason is that the gradient of the solid line is greater than that of the broken line because of loss of the electrodes of the capacitor. Q value of the capacitor was measured with a half wave length strip-line resonator and is above 80 up to 8 GHz.

Design of miniaturized balanced amplifier

The balanced amplifier circuit has a pair of "unit amplifiers" combined by 3-dB hybrid couplers at the input and output ports. The balanced amplifier configuration offers the advantage of input and output impedances equal to the characteristic impedance of a transmission line in the operating frequency range. This means that direct interconnection of these amplifiers is possible for forming a multi-stage amplifier chain without any readjustment. The bias voltage is supplied from a high impedance circuit not to affect the performance of the amplifier. Therefore, a matching circuit can be designed independent of bias circuit. To design input and output matching circuits, s-parameters of a GaAs FET chip were measured using an automatic network analyser. The circuit elements, required to achieve the desired performance with stable operating conditions, were determined using a program for computerized optimization of microwave amplifier circuits(COM AC).

An equivalent circuit of the unit amplifier is shown in Fig.3. To miniaturize the unit amplifier, its matching circuits have been designed as simply as possible using a computer simulation. Optimized values of the circuit elements are also shown in Fig.3. Amplifier performance is most affected by L_2 and C_2 in Fig.3. They must be closely controlled to achieve gain flatness. For example, at a frequency of 8 GHz if the value of C_2 is decreased to 20 percent below the optimized value, the gain of the amplifier is reduced by about 1 dB. The value of capacitance can be controlled within 8 percent.

Structure and performance of the amplifier

The miniaturized GaAs FET balanced amplifier, shown in Fig.4, consists of two GaAs FET chips(gate-width of $300 \mu\text{m}$), and lumped elements(inductors, capacitors, and resistors) and two 3-dB hybrid couplers fabricated on a sapphire substrate by photolithography. The amplifier circuit is designed within the $4\text{mm} \times 5\text{mm}$ dimensions of the sapphire substrate, which is mounted on a metal base.

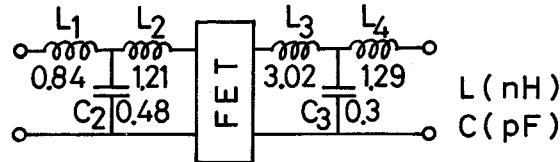


Figure 3. Equivalent circuit and optimized values of circuit elements of a "unit amplifier".

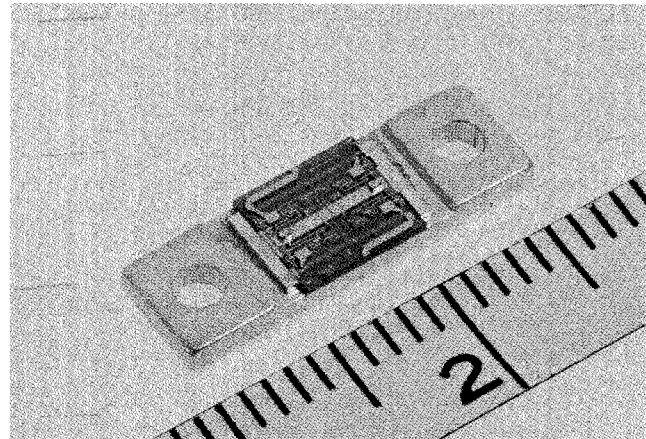


Figure 4. Photograph of the 4-8 GHz miniaturized GaAs FET balanced amplifier.

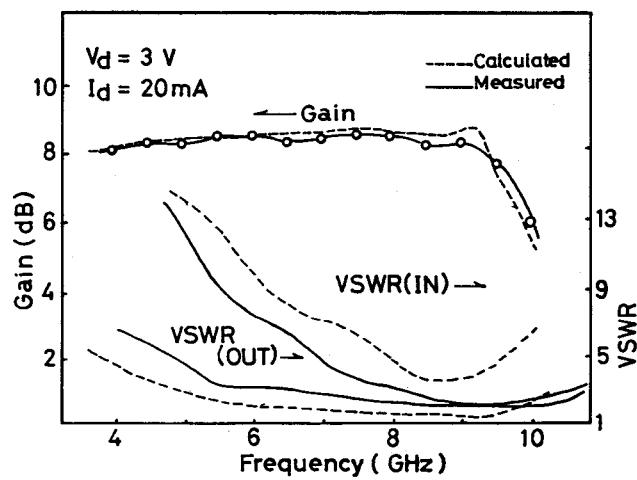


Figure 5. Calculated and measured characteristics of the unit amplifier.

In Fig.5, a broken line shows the calculated frequency response of the gain of the unit amplifier and a solid line shows that of a unit amplifier fabricated on a sapphire substrate. Coincidence of the calculated and measured values shows the effectiveness of the CAD technique.

Fig.6 shows the frequency response of the gain of a single-stage GaAs FET amplifier. This amplifier has a gain of 7.6 to 8.5 dB over the frequency range of 4 to 8 GHz at a bias current of 60 mA. Noise figure of the miniaturized balanced amplifier is 3.5 dB at the frequency of 6 GHz when a bias current of 20 mA.

Fig.7 shows the frequency response of the gain of a three-stage GaAs FET amplifier, which has a gain of 21.5 to 23.5 dB over the frequency range of 4.5 to 8 GHz at a bias voltage of 5 V and a bias current of 200 mA. The last-stage amplifier delivered the output power of 36 mW with 1-dB gain compression of 5.9 dB at 7.5 GHz.

Conclusion

A miniaturized GaAs FET balanced amplifier has been fabricated on a sapphire substrate by thin film technology. Dimension of the amplifier is as large as a quarter of conventional amplifier.

There have been many recent developments in monolithic microwave integrated circuits using GaAs substrates². The hybrid amplifier described in this paper is superior to the monolithic amplifier from the standpoint of cost vs. performance. The same techniques as described in this paper will also surely lead to the development of miniaturized high power amplifier.

Acknowledgement

The authors wish to thank Y. Fukukawa, T. Sekizawa, and H. Komizo for their encouragement and guidance. We wish to thank M. Itoh of the Semiconductor Engineering Department of Fujitsu Ltd. for supplying the GaAs FETs.

References

- 1) H.Q.Tserng et al., "Microwave GaAs Power FET Amplifier with Lumped Element Impedance Matching Networks." MTT-S International Microwave Symposium, pp.282-pp.284, June, 1978
- 2) J.A.Higgins et al., "GaAs FET Monolithic Circuits." IEEE International Solid-State Circuit Conference, February, 1979

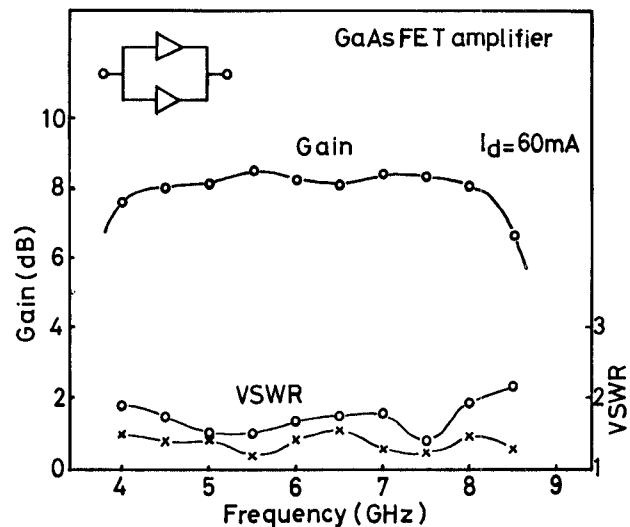


Figure 6. Frequency response of a gain of the single-stage GaAs FET amplifier.

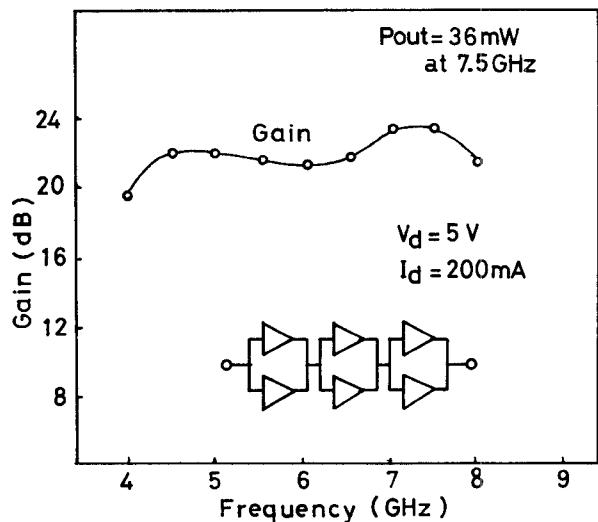


Figure 7. Frequency response of a gain of the three-stage GaAs FET amplifier.